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AF 2811

#29/Ext(1) Appeal Brief 1/30/03 ASmith

Docket No.: GR 97 P 2734

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By: [signature] Date: January 21, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applicant : Frank Hintermaier

Applic. No. : 09/161,196

Filed : September 25, 1998

Title : Capacitor Having a Barrier Layer Made of a Transition Metal Phosphide, Arsenide or Sulfide

Examiner : Cuong Q. Nguyen - Art Unit: 2811

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BRIEF ON APPEAL

Hon. Commissioner of Patents and Trademarks,
Washington, D. C. 20231,

Sir:

This is an appeal from the final rejection in the Office action dated June 4, 2002, finally rejecting claims 1, 3, 5 and 7-12.

01/30/2003 ASMITH 00000002 121099 09161196
01 FC:1251 110.00 CH

Appellants submit this *Brief on Appeal* in triplicate, accompanied by a check for $320.00 to cover the fee for filing the *Brief on Appeal*.

01/28/2003 CV0111 00000061 09161196
01 FC:1402 320.00 OP

Real Party in Interest:

This application is assigned to *Infineon Technologies AG* of Munich, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1, 3, 5 and 7-12 are rejected and are under appeal. Claims 2, 4, 6 and 13-24 are withdrawn from further consideration.

Status of Amendments:

No claims were amended after final. A response after final (37 CFR § 1.116) was filed on December 4, 2002. The response filled after final did not contain a proposed amendment either to the claims or to the specification.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention

relates to a capacitor in an integrated circuit, in particular in an integrated semiconductor memory.

Appellant explained on page 11 of the specification, line 14, that, referring to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is seen a capacitor that is used as a storage capacitor in an integrated semiconductor memory, in particular a DRAM or FRAM. The figure shows a silicon substrate 1 having, arranged on it, a MOS transistor which comprises two doped regions 3, 4 and a gate 5 that is insulated relative to the substrate. Inactive regions of the circuit are covered with an insulation 2. An insulation layer 6 covers the transistor. A structure 7 connects to the doped region 3. The other doped region 4 is connected via a further connection structure 8 to a bit line 9. In this case, the connection structure 7 consists of tungsten, with which a contact hole etched into the insulation layer 6 is filled. The insulation layer 6 may consist of silicon oxide or nitride. In order to produce the barrier layer, the existing structure is then heat-treated in a PH_3 atmosphere. The tungsten W then reacts with the PH_3, so that WP 10 is formed self-aligned on the connection structure 7. Typical parameters of the heat treatment are a temperature of from 800 to 1100°C and a pressure of from 0.1 to 10 torr PH_3. Part of the connection

structure 7 is thus converted directly into WP. The layer thickness of the barrier 10 can be adjusted through the duration of the heat treatment. A typical value for the thickness of the layer 10 is about 30 nm.

Appellant stated on page 12 of the specification, line 13, that, referring to Fig. 2, the lower electrode 11 of the capacitor is then applied, for example by sputtering an approximately 30 nm thick Pt layer and suitable structuring. After this, a high-ε dielectric 12 is deposited. During the deposition, the tungsten phosphide acts as a barrier preventing oxygen from diffusing in, and prevents oxidation of the connection structure 7. Lastly, a second electrode 13 of the capacitor is produced, for example from platinum. In the exemplary embodiment, the electrode 13 represents the so-called common plate for all the capacitors.

Appellant further outlined on page 12 of the specification, line 24, that, referring to Fig 3, the second embodiment commences with the same prefabricated basic structure as the first exemplary embodiment, that is to say a substrate having a MOS transistor which is covered with an insulation layer 6, a connection structure 7 being connected, passing through this insulation layer 6, to a doped region 3 of the transistor. The barrier layer 10 is then applied surface-

wide to this structure by CVD. To that end, a mixture of tungsten chloride (WCl_6), hydrogen (H_2) and phosphine (PH_3) is produced in a chamber. At a temperature of from 400 to 800°C and a pressure of from 0.1 to 10 torr, tungsten phosphide (WP) is deposited on the entire surface. As an alternative, tantalum phosphide may also be deposited from the starting materials $TaCl_5$, H_2 and PH_3 in a CVD process. Platinum is applied on top as the material of the lower electrode 11.

Appellant explained on page 13 of the specification, line 14, that, referring to Fig. 4, the two layers 10, 11 are structured with the aid of a photographic technique in an etching process, so as to form a first electrode 11 which then lies on the barrier layer 10. As in the first illustrative embodiment, the capacitor is fabricated by production of the capacitor dielectric 12 and of the second electrode 13.

Appellant further outlined on page 13 of the specification, line 21, that the barrier layer 10 may also be arranged on the first electrode 11. Since, in this case, it also needs to cover the sides of the first electrode, the first electrode is expediently structured initially, and then the barrier layer is applied. The first electrode and the barrier layer may, however, also be structured together,

wherein case the sides of the first electrode need to be covered, for example, by a spacer made of the material of the barrier.

References Cited:

U.S. Patent No. 5,566,045 (*Summerfelt et al.*), dated October 15, 1996;

U.S. Patent No. 5,691,219 (*Kawakubo et al.*), dated November 25, 1997;

Issues

Whether or not claim 1 is anticipated by *Summerfelt et al.* or *Kawakubo et al.* under 35 U.S.C. §102.

Grouping of Claims:

Claim 1 is independent. Claims 3, 5 and 7-12 depend on claim 1. The patentability of claims 3, 5 and 7-12 is not separately argued. Therefore, claims 3, 5 and 7-12 stand or fall with claim 1.

Arguments:

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a ***barrier layer*** disposed below said capacitor dielectric, said barrier layer consisting essentially of a compound formed from a ***transition*** element and a material selected from the group consisting of phosphorus, sulfur, and arsenic.

Claim 1 is not anticipated by *Summerfelt et al.*

On page 2 of the final Office action dated June 4, 2002, the Examiner stated that "Summerfelt et al. discloses … a GaP layer … which is a compound of a ***transition*** element (Ga)" (emphasis added).

In the *Response to Arguments* on page 4 of the Office action dated June 4, 2002, the Examiner stated that:

> Applicants [sic] argue that gallium is not a transitional element. In response, the evidence that Ga is a transitional element was already provided to Applicant in the final office action filed on 11-06-00. US patents US705685, US5990348, US6043184, and US6060419, presented

as the evidence, clearly teach that gallium is a transitional element.

US 705,685 (*Lyons*) was issued on July 29, 1902, and it pertains to telephony. US 705,685 mentions neither "transition metals" nor "Gallium", and is in a field of "telephony" which is a completely different field of technology than the field of technology of the instant application. It is assumed that either the patent number cited by the Examiner is incorrect or that the Examiner may have confused the name of the inventor Joseph Lyons of US 705,685 with the name of the (co)inventor, James E. Lyons, of US 5,990,348, US 6,043,184, and US 6,060,419.

US 5,990,348 (*Lyons et al.*) concerns the conversion of alkanes to unsaturated carboxylic acids over heteropoly acids supported on polyoxometallate salts. In column 8, lines 2-5, (similarly, column 10, lines 23-27, and column 14, lines 45-48) *Lyons et al*. state that "X is a Group IIIB, IVB, VB, VIB ***or*** transition element, such as phosphorus, silicon, gallium, aluminum, arsenic, germanium, boron, cobalt, cerium, praseodymium, uranium and thorium" (emphasis added). It is believed that the Examiner's insistence that Gallium is a transition metal is based on this passage.

However, the above-noted passage does not state that gallium is a transition metal. The list "such as phosphorus, silicon, gallium, aluminum, arsenic, germanium, boron, cobalt, cerium, praseodymium, uranium and thorium" refers to all of the terms listed before this explanatory list, i.e., groups IIIB, IVB, VB, and VIB, ***and*** transition elements, but not transition metals alone.

The same applies to the other references, US 6,060,419 (*Wijesekera et al.*) and US 6,043,184 (*Karmakar et al.*) cited by the Examiner. Both of these references use the same definition as used in US 5,990,348 (it is assumed because these references appear have the same (co)inventor).

Therefore, the Examiner's insistence that Gallium is a transition element is based on an incorrect interpretation of the above-noted passages in the US 5,990,348, US 6,060,419 and US 6,043,184. US 705,685 is of no relevance regarding the instant application.

Appellant maintains that gallium is ***not*** a transitional element and filed with the response dated October 4, 2002, copies of the relevant pages of the chemical standard work *Main Group Chemistry* (please note the title and that Ga is within the subject-matter of *Main Group Chemistry*). In particular, page 55 of *Main Group Chemistry* states that

"Group IIIB (… Ga …) would then become Group 13 because of the intervening transition metals in Groups 3-12." Appellant filed with the response dated October 4, 2002, copies of the relevant pages of the *Concise Encyclopedia of Science & Technology*. In particular, the periodic table shown on page 827 of *Concise Encyclopedia of Science & Technology* clearly illustrates that Ga is not categorized under the heading "Transition Elements" but under the heading "[group] III". Similarly, the filed periodic table reproduced from ENCYCLOPAEDIA BRITANNICA.

It is respectfully pointed out that gallium is a group IIIb element and, therefore, is not a transition element. Hence, claim 1 is not anticipated by *Summerfelt et al*..

Claim 1 is not anticipated by *Kawakubo et al*.

The Examiner states on page 3 of the Office action of the final Office action dated November 6, 2000, that:

> Kawakubo et al. does not explicitly teach that the barrier is a compound of a transitional element and phosphorous as the barrier; however, this barrier layer is taken to be inherently present in Kawakubo et al. for the following reasons: the transitional metal layer … will react with phosphorous from the connection structure … inherently forming a barrier material such as a TiP or TaP. Noted that, US 6015997 [sic] patent … provides proof for Ti or Ta will react with phosphorous in polysilicon to form TiP or TaP barrier layer in Kawakubo et al. See US6011997's col. 7 lines 50-60.

As discussed in MPEP § 2112, an element of a claim that is not expressly or implicitly disclosed in a prior art reference is inherently disclosed therein if, and only if, the "missing" element is *necessarily* present in the prior art. The principles of inherency require that the inherency be absolute, and not probabilistic.

U.S. Patent No. 6,015,997, states at col. 7, lines 55-60, that "[c]ertain Group VB nonmetal elements, such as: N, P, As, and Sb, ***can*** react with titanium to form barrier materials" (emphasis added). The word "can" is probabilistic and, hence, not absolute or certain. U.S. Patent No. 6,015,997 offer support that it is ***not*** inherent that the transitional metal layer will react with phosphorous from the connection structure, as alleged by the Examiner.

Even if for arguments shake, it is assumed that it is inherent that the transitional metal layer will react with phosphorous from the connection structure, it is not necessarily inherent, that the formed component will result in a barrier ***layer***, as recited in claim 1. U.S. Patent No. 6,015,997, does not offer support for Examiner's assertion that *Kawakubo et al.* inherently has a barrier layer of TaP or TiP.

In the *Response to Arguments* in item 2 on page 4 of the Office action dated June 4, 2002, the Examiner stated that: "Applicants argue that the concentration of phosphorous atoms used as a dopant for a plug is far too low to create a TiP barrier layer. In response, the arguments of counsel cannot take the place of evidence in the record." In view of the Examiner's response, Appellant filed with the response dated October 4, 2002, a *Declaration under 37 C.F.R. § 1.132* declaring that "the concentration of phosphorous atoms used as a dopant for a plug is far too low to create a TiP barrier layer in case only titanium and no additional phosphorous atoms are present." (Counsel telephoned the Examiner on September 26, 2002, and discussed with the Examiner the above-noted declaration. Counsel's understanding of the telephone conversation with the Examiner was that the Examiner will consider the declaration in spite of being filed in response to a final Office action.)

Hence, it is believed that it is not inherent that the transitional metal layer will (i) ***necessarily react*** with phosphorous from the connection structure to form (ii) a ***barrier*** layer. Therefore, claim 1 is not believed to be anticipated by *Kawakubo et al*.

Consequently, it is believed that neither *Summerfelt et al.* nor *Kawakubo et al.* show a ***barrier layer*** formed from a ***transition*** element and a material selected from the group consisting of phosphorus, sulfur, and arsenic, as recited in claim 1 of the instant application.

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

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Appendix - Appealed Claims:

1. A capacitor in an integrated semiconductor circuit, comprising:

a semiconductor substrate having a doped region formed therein;

a first electrode connected to said doped region;

a second electrode;

a capacitor dielectric insulating said first electrode from said second electrode; and

a barrier layer disposed below said capacitor dielectric, said barrier layer consisting essentially of a compound formed from a transition element and a material selected from the group consisting of phosphorus, sulfur, and arsenic.

3. The capacitor according to claim 1, which further comprises a connection structure connecting said first electrode to said doped region.

5. The capacitor according to claim 3, wherein said barrier layer is disposed underneath said first electrode and covers an entire interface between said first electrode and said connection structure.

7. The capacitor according to claim 1, wherein said capacitor dielectric consists of a material selected from the group consisting of dielectric material and ferroelectric material, and has a value of $\varepsilon > 100$.

8. The capacitor according to claim 1, wherein said capacitor dielectric consists of a material selected from the group consisting of BST, SBT, PZT, and PLT.

9. The capacitor according to claim 1, wherein said first electrode consists of a material selected from the group consisting of Pt-containing material, Ru-containing material, Rh-containing material, and Ir-containing material.

10. The capacitor according to claim 3, wherein said connection structure is made of a material selected from the group consisting of polysilicon and tungsten.

11. The capacitor according to claim 1, wherein said barrier layer is essentially a layer selected from the group consisting of a tungsten phosphide layer, a tantalum phosphide layer, and a hafnium phosphide layer.

12. A semiconductor configuration, comprising a capacitor according to claim 1, and an associated selection transistor which encompasses said doped region.